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PATENT
Attorney Docket No. ASC-044

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

COPY OF AMDT. IN RESPONSE TO NON FINAL REJECTION,

APPLICANT(S):	Eugene A. Fitzgerald et al.	RECEIVED ON
SERIAL NO.:	09/884,172	GROUP NO.:
FILING DATE:	June 19, 2001	EXAMINER:
TITLE:	METHOD OF FABRICATING CMOS INVERTER AND INTEGRATED CIRCUITS UTILIZING STRAINED SILICON SURFACE CHANNEL MOSFETS	

Commissioner for Patents
Washington, D.C. 20231AMENDMENT AND RESPONSE

Sir:

This is an amendment to the above-identified application in response to the Office
Action mailed on September 24, 2002.

In the Claims

Please cancel claims 2, 3, 14, and 15, and amend the claims in accordance with
the clean and marked-up versions that accompany this paper.

REMARKS

In the Office Action mailed on September 24, 2002, the Examiner rejected claims
1-3, 5-15, and 17-25 as obvious over Rim et al.; and claims 1, 4, 13, and 16 as
unpatentable over Rim et al. in view of Chu et al. The Examiner's allowance of claims
26 and 27 is noted with appreciation.

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We have amended claims 1 and 13 to specify planarization of an intermediate layer to a specified roughness level. As explained on page 9, lines 4-5 of the specification, flattening the surface to the specified degree results in "high quality material ... well suited for state of the art CMOS processing."

We submit that neither cited reference discloses or even suggests planarization, or the benefits of the recited roughness level to CMOS devices and processing techniques.

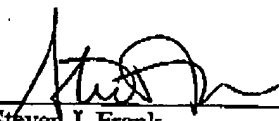
Accordingly, we submit that all claims are now in condition for allowance.

Please charge any fee occasioned by this paper to our Deposit Account No. 20-0531.

Respectfully submitted,

Date: December 1, 2002
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